AMENDMENTS TO THE DRAWINGS

The attached replacement drawing sheets include changes to Figures 1A-1B as set forth in the Remarks portion of this paper.

Attachments: Replacement sheets containing amended Figures 1A-1B.

REMARKS

Claims 1, 14 and 26 have been amended. Claims 1-3, 6-11, 14-16, 20, 22-24, 26-33 and 52-54 are pending. Applicant reserves the right to pursue the original and other claims in this and in other applications.

The drawings stand objected to. Figures 1A and 1B have been amended to include the legend "PRIOR ART." Applicant respectfully submits that the objection be withdrawn.

Claims 1-3, 6, 7, 10, 11, 14-16, 20, 24, 26-29, 32, 33 and 52-54 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over alleged Applicant's Admitted Prior Art ("AAPA") in view of JP 63-9968 ("Yoshinori"). Applicant respectfully traverses the rejection.

Claim 1 recites an image sensor comprising "a substrate formed over a base layer; a plurality of pixel cells formed within said substrate, each pixel cell comprising a photo-conversion device having a charge collection region of a second conductivity type for accumulating photo-generated charge formed in said substrate below a first layer of a first conductivity type; and a plurality of trenches, each trench being provided along a perimeter of a respective pixel cell, each trench extending at least to a surface of the base layer and below a lower level of said photo-conversion device, each trench having sidewalls, and being at least partially filled with a material that inhibits electrons from passing through said trench, wherein each of said plurality of trenches prevents diffusion of photo-generated charge generated by said photo-conversion device in one pixel cell to an adjacent pixel cell." Yoshinori does not teach or suggest all of the limitations of claim 1.

The claimed invention relates to a deep trench isolation structure and method for reducing crosstalk among semiconductor circuits and particularly, among adjacent photodiodes formed in pixel circuits. In one embodiment, a trench is etched into a substrate adjacent to a photodiode region, wherein the trench extends to an epitaxial layer below the substrate. (Present Application, ¶ [0011]). The deep trench inhibits electrons from diffusing under the isolation trench to an adjacent pixel. (Present Application, ¶[0031]). Yoshinori and the AAPA fail to teach or suggest the claimed invention.

Applicant submits that if the document is in a language other than English and the examiner seeks to rely on that document, a translation must be obtained so that the record is clear as to the precise facts the examiner is relying upon in support of the rejection. *See* MPEP § 706.02. The record must also be clear as to whether the examiner is relying upon the abstract or the full text document to support a rejection. *See* MPEP § 706.02. The Office Action does not include a full English translation of Yoshinori, but only an English translation of the abstract. The Office Action cites to Figures 1-7 and particularly to Figure 6 of Yoshinori to contend that Yoshinori discloses all of the limitations of claim 1. (Office Action, p.3). But the Office has failed to satisfy its burden, under a §103(a) rejection, as it has failed to specifically provide and identify elements of Yoshinori that disclose or teach the claimed invention. Specifically, Figures 6 and 7 relied upon by the Office Action are not described in the English language Abstract provided by the Examiner. Accordingly, the rejection of claim 1 and its dependent claims 2-3, 6, 7, 10, 11 and 52-54 should be withdrawn for at least this reason. Claims 14-16, 20, 24, 26-29, 32 and 33 contain similar limitations as claim 1 and therefore, the rejection of these claims should also be withdrawn.

In any event, an English translation of Yoshinori (obtained by the Applicant and a copy of the relevant page discussing Figure 6 which is enclosed herewith) reveals that Yoshinori does not disclose, teach or suggest all of the limitations of claim 1. Figure 6 of Yoshinori shows that the pinphotodiode consists of diffusion layer 4, epitaxial layer 2 and substrate 1. (second full paragraph of Yoshinori translation). The Yoshinori trench stops at the substrate 1. Thus, the trench 3 in Yoshinori Figure 6 is not below a lower level of the Yoshinori pinphotodiode. Particularly, Yoshinori does not disclose or teach "each trench extending at least to a surface of the base layer and below a lower level of said photo-conversion device." Therefore, Applicant respectfully requests that the rejection of independent claim 1 and its dependent claims 2-3, 6, 7, 10, 11 and 52-54 be withdrawn and the claims allowed.

Claim 14 recites a structure for isolating an active area on a semiconductor device comprising, in part, "a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, wherein said trench extends at least to a surface of a base layer below said substrate which is below a lower level of said photo-conversion device, and wherein said trench has sidewalls." For the above-mentioned reasons, claim 14 and its dependent claims 15-16, 20 and 24 are likewise allowable.

Claim 26 recites a processor system comprising, in part, "a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, the active area having a photo-conversion device comprising a charge collection region of n-type conductivity for accumulating charge and located below a p-type region of said active area, wherein said trench extends at least to a surface of a base layer below said substrate and to a level below a lower level of said photo-conversion device, and

wherein said trench has sidewalls and inhibits diffusion of charge outside said active area." For the above-mentioned reasons, claim 26 and its dependent claims 27-29, 32 and 33 are likewise allowable.

Claims 8, 9, 22, 23, 30 and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over alleged AAPA in view of Yoshinori and US 2004/0227061 ("Clevenger"). Applicant respectfully traverses the rejection.

Claims 8 and 9 depend from claim 1 and as such, recite an image sensor, comprising, in part, "a photo-conversion device having a charge collection region of a second conductivity type for accumulating photo-generated charge formed in said substrate below a first layer of a first conductivity type; and a plurality of trenches, each trench being provided along a perimeter of a respective pixel cell, each trench extending at least to a surface of the base layer and below a lower level of said photo-conversion device, each trench having sidewalls, and being at least partially filled with a material that inhibits electrons from passing through said trench, wherein each of said plurality of trenches prevents diffusion of photo-generated charge generated by said photo-conversion device in one pixel cell to an adjacent pixel cell."

Claims 22 and 23 depend from claim 14 and as such, recite a structure for isolating an active area on a semiconductor device comprising, in part, "a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, wherein said trench extends at least to a surface of a base layer below said substrate which is below a lower level of said photo-conversion device, and wherein said trench has sidewalls."

Claims 30 and 31 depend from claim 26 and as such, recite a processor system comprising, in part, "a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, the active area having a photo-conversion device comprising a charge collection region of n-type conductivity for accumulating charge and located below a p-type region of said active area, wherein said trench extends at least to a surface of a base layer below said substrate and to a level below a lower level of said photo-conversion device, and wherein said trench has sidewalls and inhibits diffusion of charge outside said active area."

As mentioned earlier, Yoshinori fails to teach or disclose all of the limitations of claims 1, 14 and 26. Clevenger fails to cure the deficiencies of Yoshinori. The Office Action relies on Clevenger to only teach a trench depth greater than about 2000 Angstroms and a CMOS image sensor. (Office Action, pp. 8-9). Therefore, Applicant respectfully requests that the rejection of claims 8, 9, 22, 23, 30 and 31 be withdrawn and the claims allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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体撮像素子の応用分野はホームビデオカメラに限らず、視覚センサとして工業用ロボット,防犯カメラ、天文観測、スチルカメラ等の多方面に広がっている。かかる固体撮像素子に対する要求項目の一つに高感度化がある。スチルカメラの実用化,映像の高品質化,ビデオカメラの超小型化に対する強いニーズに応えるためには、撮像素子の高感度化が必須の要件になっている。

d to market . applied field of solid state camera element is spreading to industrial robot , crime prevention camera , astronomical observationand still camera or other polyhedron not just home video camera , as visual sensor . There is a increasing sensitivity in one of requirement for this solid state camera element . In order to answer to strong needs where it confronts ultraminiaturization of quality increase , video camera of utilization and image of still camera , increasing sensitivity of the photographic element has become necessary requisite .

SITを光電変換素子として用いるラインセンサや固体撮像素子は、光電荷を素子内部で増幅できるため、高感度イメージセンサとしての期待が持たれている。第6図はSITイメージセンサが高感度であることに着目して、1つのセル寸法を縮小し、微細なセルで構成したSITイメージセンサのセルの断面を示す図であり、n'基板1をドレインとし、その上に成長させたn-エピタキシャル層2内にトレンチ分離部3で分離されたSITセルI,II,III がアレイ状に配置されている状態を示している.1つのセルはp'拡散層4で形成されるゲート、浅いいn'拡散層5で形成されるソース、及びゲート容量を形成するための薄いゲート酸化膜6 及び該酸化膜 6 上に形成されたポリシリコン7、並びにソースを形成するn'拡散層5からコンタクトを取るためのポリシリコン 8 からなっている。そしてゲート酸化膜6,ソ-ス拡散層5 以外のシリコン表面は厚い酸化膜9で覆われている。

As for line sensor and solid state camera element which use SIT as photoelectric conversion element , the photo charging amplifying because it is possible with element interior , expectation as high sensitivity image sensor leans. Figure 6 paying attention to SITimage sensor being high sensitivity , reduces the cell dimension of one , in figure which shows cross section of cell of SITimage sensor which configuration is done, designates n'substrate 1 as the drain with microscopic cell , In order to form source , and gate capacity which as for cell ofthe.one which has shown state where SITcell I, II, III which is separatedinside n- epitaxial layer 2 which grew on that in trench isolation section 3 is arranged in array gate , which is formed with p'diffusion layer 4 it is shallow areand are formed with n'diffusion layer 5 thin gate oxide film 6 and It has consisted of polysilicon 8 in order to take contact from the polysilicon 7, which was formed on said oxide film 6 and n'diffusion layer 5 which forms the source . And as for silicon surface other than gate oxide film 6, source diffusion layer 5 it is covered with thick oxide film 9.

このように構成されている SIT セルにおける光電変換は、p'ゲート拡散層4,n-エピタキシャル層2,n'ドレイン基板1からなるpinホトダイオードで行われる.光蓄積期間に、このホトダイオードは逆バイアスされ、光入射によって発生する電子はn'ソ-ス拡散層5かn'ドレイン基板1へ逃げ、ホールはp'浮遊ゲート拡散層4に蓄積され、ゲート電位を上昇する.そして光電荷によるゲート電位の増加分が、光信号読み出し期間中に、ポリシリコン7,ゲート酸化膜6p'ゲ-ト拡散層4からなるゲート容量を介してp'ゲート拡散層4に加えられるゲートバイアス電圧に加算されるため、ソ-ス拡散層5とドレイン基板1との間には光電荷の蓄積量に対応する大きな出力電流が流れ、光信号が読み出される。SIT イメージセンサのセル構成は、光電変換と増幅作用とが1つのSIT内で行われるため、1つのセル当たり1個のトランジスタでよく、微細化には適している。SITイメージセンサの微細化を行うには、素子分離領

this way as for photoelectric conversion in SITcell which configuration is done,in the.optical storage time which is done with pinphotodiode which consists of p'gate diffusion layer 4, n- epitaxial layer 2, n'drain substrate 1,as for this photodiode reverse bias it is done, electron which occurs withoptical incidence escapes to n'source diffusion layer 5 or n'drain substrate 1, hole the compilation is done in p' floating gate diffusion layer 4, gate voltage rises. And with photocharging increased fraction of gate voltage , in light signal reading time , polysilicon 7, gate oxide film 6p' [ge] - through gate capacity which consists of * diffusion layer 4,because it is added to gate bias voltage which is added to p'gate diffusion layer 4,corresponds to stored amount of photocharging between source diffusion layer 5 and drain substrate 1 large output current to flow, light signal reads out. cell configuration of SITimage sensor , because photoelectric conversion and amplifying action are doneinside SIT of one , may be transistor of per cell 1 of the one , suitable for narrowing